REMARKS

The present Amendment amends claims 1, 8, 9, and 12, and cancels claims 2-7 10, 11, and 13-20. Therefore, the present application has pending claims 1, 8, 9, and 12.

Information Disclosure Statement

The Examiner objected to the Information Disclosure Statement filed on July 7, 2003 because all of the foreign references were not accompanied by English-language abstracts or translations. Applicants are filing herewith an Information Disclosure Statement including English-language abstracts for the references not yet considered by the Examiner.

Title

The Examiner objected to the title of the invention, asserting that a new title is required that is clearly indicative of the invention to which the claims are directed. Applicants have amended the title to overcome this objection. Therefore, this objection should be withdrawn.

Drawings

The Examiner objected to the drawings because reference character "170" has been used to designate two different features shown in Fig. 10. Applicants have amended Fig. 10 to overcome this objection. Therefore, this objection should be withdrawn.

Specification

The Examiner objected to the specification, citing informalities. Where appropriate, Applicants have amended the specification to overcome these objections. Therefore, this objection should be withdrawn.

Claim Objections

The Examiner objected to claim 7, citing antecedent basis problems. As indicated above, claim 7 was canceled. Therefore, this objection is rendered moot.

35 U.S.C. §102 Rejections

Claims 1-6 and 10-20 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,948,053 to Augsburg, et al. ("Augsburg"). As indicated above, claims 2-6, 10, 11, and 13-20 were canceled. Therefore, this rejection with regard to claims 2-6, 10, 11, and 13-20 is rendered moot. This rejection with regard to the remaining claims 1 and 12 is traversed for the following reasons. Applicants submit that the features of the present invention, as now more clearly recited in claims 1 and 12, are not taught or suggested by Augsburg, whether taken individually or in combination with any of the other references of record. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

Amendments were made to the claims to more clearly describe features of the present invention. Specifically, amendments were made to the claims to more clearly describe that the present invention is directed to a data processing device as recited, for example, in independent claim 1.

The present invention, as recited in claim 1, provides a data processing device that decodes and executes instructions, which contain a spare field. The data processing device includes an instruction cache memory, a predecode-processor, and an instruction flow unit. The predecode-processor decodes operation codes contained in first fields of each of the instructions, so as to generate a piece of information. The information represents whether the instruction is a branch instruction or not. The predecode-processor also transfers the information as the spare field of each of the instructions. The instruction flow unit controls an executing sequence of the instructions based on information of the spare field, when executing instructions loaded from the cache memory. Also in the data processing device, the instruction flow unit issues commands to fetch an instruction of a branch destination, when it determines that the instruction is a branch instruction, based on the information of the spare field. The prior art does not disclose all these features.

The above described features of the present invention, as now more clearly recited in the claims, are not taught or suggested by any of the references of record, particularly Augsburg, whether taken individually or in combination with any of the other references of record.

Augsburg discloses a method and system for calculating a branch target address. However, there is no teaching or suggestion in Augsburg of the data processing device of the present invention, as recited in the claims.

In Augsburg's method and system for calculating a branch target address, a branch instruction is fetched from memory. Upon fetching the branch instruction the

n-1 lower order bits of the branch target address may be pre-calculated and stored in the branch instruction prior to storing the branch instruction in the instruction cache. Upon retrieving the branch instruction from the instruction cache, the upper order bits of the branch target address may be recovered using the sign bit and the carry bit stored in the branch instructing. The sign bit and the carry bit may be used to select one of three possible upper-order bit combinations of the branch target address. The selected upper-order bit value combination may then be appended to the n-1 lower order bits of the branch target address to form the complete branch target address.

One feature of the present invention, as now more clearly recited in claim 1, includes a predecode-processor that decodes operation codes contained in first fields of each of the instructions to generate a piece of information. The information represents whether or not the instruction is a branch instruction. The predecode-processor also transfers the information as the spare field of each of the instructions. Augsberg does not disclose this feature. To support the assertion that Augsburg discloses a predecode-processor that decodes operation codes contained in first fields of each of the instructions to generate a piece of information, where the information represents whether or not a the instruction is a branch instruction, the Examiner cites Fig. 2, item 202 and column 5, lines 46-64 (see paragraph 14). The Examiner further asserts that "the presence of the carry bit indicates a branch instruction, as no other type of instruction uses the spare field in predecoding." However, contrary to the Examiner's assertions, the carry bit, as shown in Fig. 6,

item 601, does not provide an indication of whether or not an instruction is a branch instruction or not, in the manner claimed.

First, as indicated in column 2, lines 48-62, and as further indicated column 9, line 4 to column 10, line 9, Augsburg discloses where based on the binary value of the sign bit and the carry bit in the relative branch instruction, the decode/selecting logic unit selects a value from the upper bits of the address of the relative branch instruction. This selection may then be appended to the n-1 significant bits of the target address to form a complete target address. As such, the carry bit is does not provide an indication as to whether or not an instruction is a branch instruction, but rather is used to make a selection that can be appended to form a complete target address.

Next, the Examiner asserts that the encoding logic unit of Augsburg, as shown in Fig. 2, item 202, is equivalent to the predecode-processor of the present invention. This is clearly incorrect in that an encoding logic unit provides encoding functions (see column 5, lines 46-64), while the predecode processor of the present invention provides decoding functions. Furthermore, as described in column 8, lines 54-57, the encoding logic unit 202 may be configured to determine if the fetched instruction is a relative branch instruction by reading the operation code of the fetched instruction. This is different from the present invention, where the predecode-processor decodes operation codes to generate a piece of information, where the information represents whether or not the instruction is a branch

instruction, and where the predecode-processor transfers the information as the spare field of each of the instructions, in the manner claimed.

Further, as described in column 12, lines 22-25, the decode/selecting logic unit (Fig. 2, item 204) of Augsburg may be configured to determine if the instruction is a relative branch instruction by reading the operation code of the instruction. This is quite different from the present invention, where the predecode-processor decodes operation codes contained in first fields of the instructions to generate a piece of information, the information representing whether or not the instruction is a branch instruction.

Therefore, Augsburg fails to teach or suggest "a predecode-processor which decodes operation codes contained in first fields of each of said instructions to generate a piece of information, said information representing whether said instruction is a branch instruction or not, and transfers the information as said spare field of each of said instructions" as recited in claim 1.

Therefore, Augsburg fails to teach or suggest the features of the present invention, as now more clearly recited in the claims. Accordingly, reconsideration and withdrawal of the 35 U.S.C. §102(e) rejection of claims 1, 8, 9, and 12 are respectfully requested.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the reference used in the rejection of claim 1.

35 U.S.C. §103 Rejections

Claim 7 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Augsburg in view of U.S. Patent No. 4,912,635 to Nishimukai, et al. ("Nishimukai"). As indicated above, claim 7 was canceled. Therefore, this rejection is rendered moot.

Claims 8 and 9 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Augsburg in view of Nishimukai, further in view of U.S. Patent No. 6,499,712 to Irie, et al. ("Irie"). This rejection is traversed for the following reasons. Applicants submit that claims 8 and 9 are dependent on claim 1. Therefore, claims 8 and 9 are allowable for at least the same reasons previously discussed regarding independent claim 1. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

In view of the foregoing amendments and remarks, Applicants submit that claims 1, 8, 9, and 12 are in condition for allowance. Accordingly, early allowance of claims 1, 8, 9, and 12 is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 C.F.R. §1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to

the deposit account of Mattingly, Stanger, Malur & Brundidge, P.C., Deposit Account No. 50-1417 (referencing attorney docket no. H-1098).

Respectfully submitted,

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Attachment: Replacement Sheet
Annotated Sheet Showing Changes

Amendments to the Drawings

The attached sheet of drawings includes changes to Fig. 10. In Fig. 10, reference numeral "170" for Data Array is changed to --171--.

Annotated Marked Up Drawings

FIG.10